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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/685,192 | 10/11/2000 | Anders Johnson | 108339-00031 | 5268 |

32294 7590 10/13/2005

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

| EXAMINER | |
|---|---|
| HA, LEYNNA A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2135 | |

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| **Advisory Action Before the Filing of an Appeal Brief** | **Application No.** 09/685,192 | **Applicant(s)** JOHNSON, ANDERS | |
|---|---|---|---|
| | **Examiner** LEYNNA T. HA | **Art Unit** 2135 | |

***--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

THE REPLY FILED 26 September 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, ~~the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended~~.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-4, 7-17, 19-23, 27-29.
   Claim(s) withdrawn from consideration: _____.

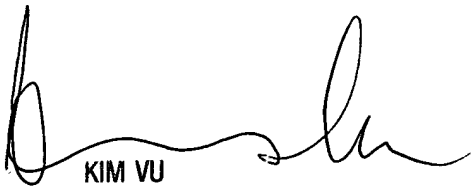
AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Continuation of 11. does NOT place the application in condition for allowance because: Claims 1-4, 7-17, 19-23, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tello (US 6,463,537) and further view in view of Angelo, et al. (US 6,370,649).
The Examiner finds that the OR gate is inherently known for controlling access to privileged functions and to switch tasks. Hence, Tello discloses a selecting device that comprises the OR gate having at least one input for receiving functions such as the function enable output and the bonding option output. Applicant argues that the enablement and disablement is dependent on whether the line is set to High or Low.
However, does not depend on what else the prior art teaches outside of applicant's claimed invention and as long as the prior art teaches what is claimed. Tello teach a selecting device as the control line (PIDEMIST_CTRL) is used to disable or enable the Primary Master IDE slot. The PIDEMIST_CTRL logically connects to the programmable device which is connected to the security engine microprocessor and the OR gate which is connected to the AND gate which in turn is connected through a Slave line to the data switch IC (COL.13, lines 15-17) and connected to the control line between the OR gate which is connected to the AND gate and the programmable device is the pull up resistor (COL.13, lines 56-58) of which the switch and the pull up resistor makes the bonding option output. Therefore, Tello has the capability to set the control line to HIGH or LOW wherein having the selecting device to either disable the line or enable the line to allow the motherboard microprocessor to recognize a device connected to the Primary Slave IDE slot (COL.13, lines 59-67) that comprises an OR gate for receiving the function enable output and the bonding option output.
To clarify the inherent functions of the OR gate, the Examiner points to the Microsoft Computer Dictionary. According to the Microsoft Computer Dictionary, a gate is an electronic switch that produces an electrical output signal that represent a binary 1 or 0 and is released to the states of one or more input signals by an operation of Boolean logic and is a data structure used to control access to privileged functions, to change data segments, or to switch tasks (pg.232). The term, "OR gate" is defined as one of the three basic logic gates from which all digital systems can be built and the output of an OR circuit is true (1) if any input is true (pg.381). Therefore, it is inherent the selecting device comprises the OR gate is used to control access to privileged functions, to change data segments, or to switch tasks. Thus, the selecting device of Tello can disable or enable the line to allow the motherboard microprocessor to recognize the device connected to the Primary Slave IDE slot because of the OR gate which controls access to privileged functions and able to switch tasks.



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